

WHAT IS CLAIMED IS:

1 1. An integrated circuit comprising a high voltage transistor on a
2 semiconductor, the high voltage transistor comprising:
3 a source formed in the semiconductor;
4 a drain formed in the semiconductor; and
5 a channel between the source and the drain,
6 wherein the drain comprises a first drain extension region, a second drain
7 extension region, and a third drain region, a concentration of majority charge carriers in the drain
8 increasing farther away from the channel at junctions between the three drain regions.

1 2. The integrated circuit of claim 1, further comprising:
2 a gate formed in a ring structure that encloses the drain.

1 3. The integrated circuit of claim 1, further comprising:
2 a gate formed into a striped structure.

1 4. The integrated circuit of claim 1, further comprising:
2 a gate shield formed partially over a gate and the drain.

1 5. The integrated circuit of claim 1 wherein the drain further comprises:
2 a fourth drain region adjacent to the third drain region that has a concentration of
3 majority charge carriers that is greater than the concentration of majority charge carriers in the
4 first, second, and third drain regions, and wherein the third drain region is a third drain extension
5 region.

1 6. The integrated circuit of claim 5 further comprising:
2 a fifth drain region adjacent to the fourth drain region that has a concentration of
3 majority charge carriers that is greater than the concentration of majority charge carriers in the
4 first, second, third, and fourth drain regions, wherein the fourth drain region is a fourth drain
5 extension region.

1 7. The integrated circuit of claim 1 further comprising:
2 a first doped well;

3 the first drain extension region comprising a region where part of the first doped
4 well overlaps part of a first doped region;
5 a second doped well; and
6 the second drain extension region comprising a region where part of the second
7 doped well overlaps part of the first doped region.

1 8. The integrated circuit of claim 7 further comprising:
2 a third doped well;
3 the third drain region comprising a third extension region formed where part of
4 the third doped well overlaps part of the first doped region; and
5 a fourth drain region that comprises a low resistance drain contact region.

1 9. The integrated circuit of claim 7 further comprising:
2 a third doped well;
3 the third drain region comprising a third extension region formed where part of
4 the third doped well overlaps part of the first doped region;
5 a fourth drain extension region; and
6 a fifth drain region that comprises a drain contact region.

1 10. The integrated circuit of claim 9 further comprising:
2 a fourth doped well;
3 the fourth drain extension region formed where a portion of the fourth doped well
4 overlaps part of the first doped region.

1 11. The integrated circuit of claim 8 wherein,
2 P-type dopant is diffused into the first doped well,
3 P-type dopant is diffused into the second doped well,
4 N-type dopant is diffused into the third doped well, and
5 N-type dopant is diffused the first doped region.

1 12. A high voltage transistor formed on a semiconductor, the transistor
2 comprising:
3 a gate formed on the semiconductor;

4 a source formed in the semiconductor; and
5 a drain formed in the semiconductor, wherein the drain comprises at least four
6 doped drain regions,
7 the four doped drain regions having a gradient of majority charge carriers
8 that laterally increases farther away from the gate across three junctions between the four drain
9 regions.

1 13. The high voltage transistor of claim 12 wherein a first drain extension
2 region comprises a portion of a first well that overlaps a first doped region,
3 a second drain extension region comprises a portion of a second well that overlaps
4 the first doped region,
5 a third drain extension region comprises a portion of the first doped region; and
6 a fourth drain region comprises a drain contact region.

1 14. The high voltage transistor of claim 13 wherein the third drain region
2 comprises a portion of a third well that overlaps the first doped region.

1 15. The high voltage transistor of claim 13 wherein,
2 P-type dopant is diffused into the first well,
3 P-type dopant is diffused into the second well, and
4 N-type dopant is diffused the first doped region.

1 16. The high voltage transistor of claim 12 wherein the drain comprises:
2 a first drain extension comprising a portion of a first well that overlaps a first
3 doped region,
4 a second drain extension comprising a portion of a second well that overlaps the
5 first doped region,
6 a third drain extension comprising a portion of a third well that overlaps the first
7 doped region;
8 a fourth drain extension region; and
9 a fifth drain region that comprises a drain contact region.

1 17. An integrated circuit comprising at least one high voltage transistor
2 formed on a semiconductor, said transistor comprising:
3 a source formed in the semiconductor; and
4 a drain formed in the semiconductor, wherein the drain comprises a first portion of
5 a first doped region that overlaps a first doped well, a second portion of the first doped region
6 that overlaps a second doped well, and a drain contact region.

1 18. The integrated circuit of claim 17 wherein the drain further comprises a
2 third portion of the first doped region that overlaps a third doped well, wherein the third portion
3 of the first doped region has a concentration of majority carriers that is greater than the
4 concentration of majority carriers in the first and the second portions of the first doped region.

1 19. The integrated circuit of claim 18 wherein the drain further comprises a
2 fourth portion of the first doped region that overlaps a fourth doped well, wherein the fourth
3 portion of the first doped region has a concentration of majority carriers that is greater than the
4 concentration of majority carriers in the third portion of the first doped region.

1 20. The integrated circuit of claim 17 wherein the transistor is an NMOS
2 transistor,
3 the first doped region of the drain is doped with N-type dopant,
4 the first doped well is doped with P-type dopant, and
5 the second doped well is doped with N-type dopant.

1 21. The integrated circuit of claim 17 wherein the drain further comprises:
2 a third portion of the first doped region that overlaps a third doped well, and
3 wherein the concentration of majority charge increases across junctions between
4 the three portions of the first doped region moving laterally away from a gate of the transistor.

1 22. The integrated circuit of claim 21 wherein the drain further comprises:
2 a fourth portion of the first doped region, and
3 wherein the concentration of majority charge increases across junctions between
4 the four portions of the first doped region moving laterally away from a gate of the transistor.

1 23. The integrated circuit of claim 17 wherein the transistor is an NMOS or a
2 PMOS device.

1 24. The integrated circuit of claim 17 wherein a concentration of majority
2 charge carriers increases laterally away from a channel of the transistor across junctions between
3 each doped region of the drain.

1 25. A high voltage transistor formed on a semiconductor, the transistor
2 comprising:
3 a gate formed on the semiconductor;
4 a source formed in the semiconductor; and
5 a drain formed in the semiconductor, wherein the drain region has a graded
6 concentration of first majority charge carriers that increases across junctions between a first drain
7 extension, a second drain extension, and a third drain region moving laterally farther away from
8 the gate, and

9 wherein a concentration of second charge carriers in a region beneath the drain
10 decreases moving laterally farther away from the gate to underneath the third drain region, the
11 second charge carriers being of the opposite doping type as the first majority charge carriers.

1 26. The high voltage transistor of claim 25 further comprising:
2 a first doped well;
3 the first drain extension comprising a region where part of the first doped well
4 overlaps part of a first doped region;
5 a second doped well; and
6 the second drain extension comprising a region where part of the second doped
7 well overlaps part of the first doped region.

1 27. The high voltage transistor of claim 26 further comprising:
2 a third doped well;
3 the third drain region comprising a third drain extension region formed where part
4 of the third doped well overlaps part of the first doped region;
5 a fourth drain extension region; and

6 a fifth drain region that comprises a drain contact region.

1 28. The high voltage transistor of claim 25 wherein the third drain region
2 comprises a low resistance drain contact region.

1 29. The high voltage transistor of claim 26 further comprising:
2 a third doped well;
3 the third drain region comprising a third drain extension formed where part of the
4 third doped well overlaps part of the first doped region; and
5 a fourth drain contact region.